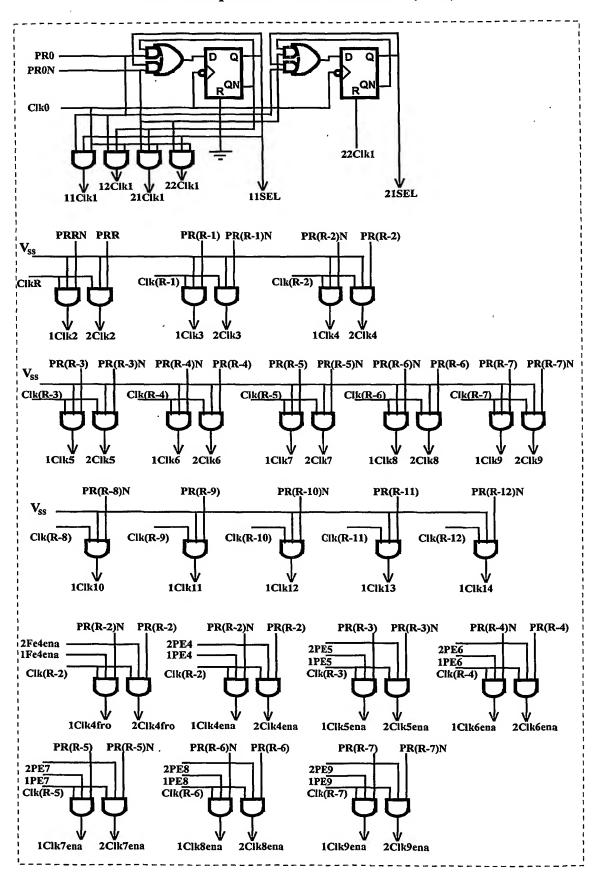


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FIG.2A Sequential Clocks Generation (SCG)



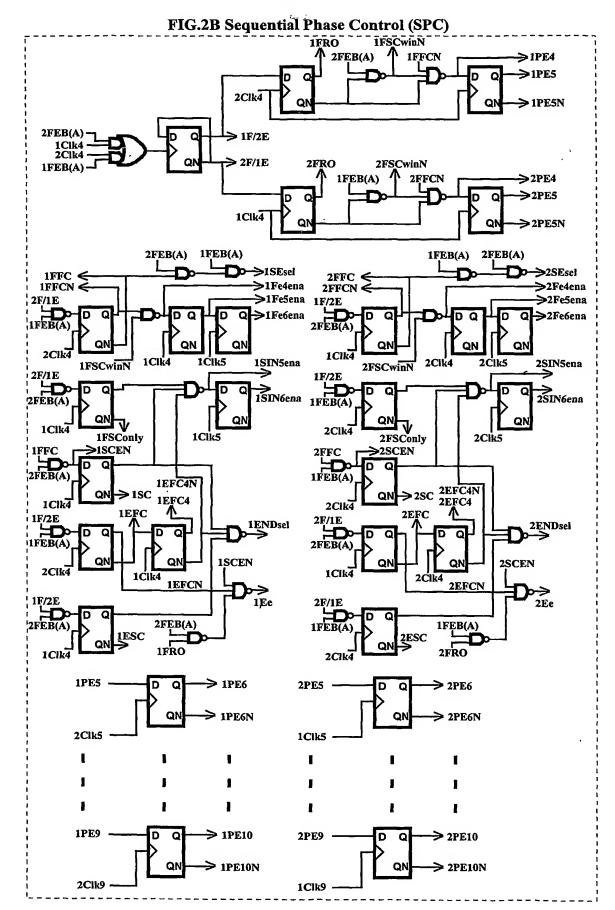
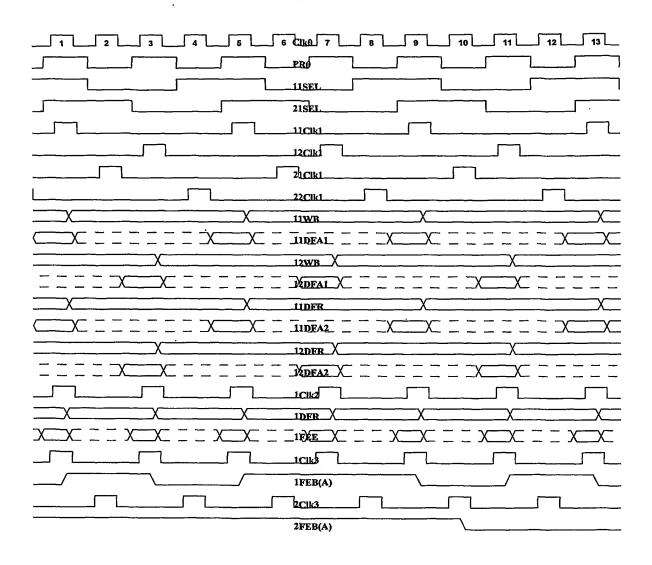
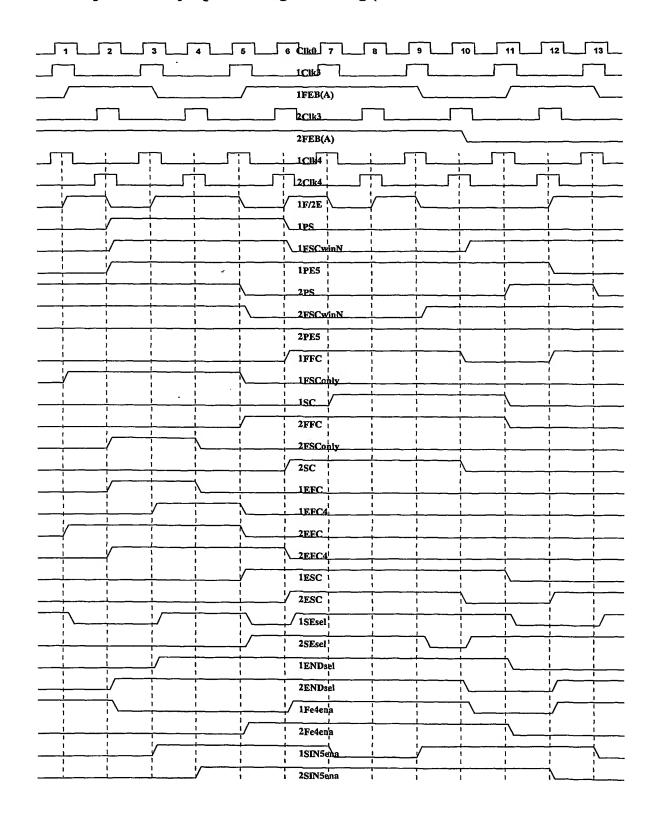


FIG.2C Timing Diagram of the SC and WC



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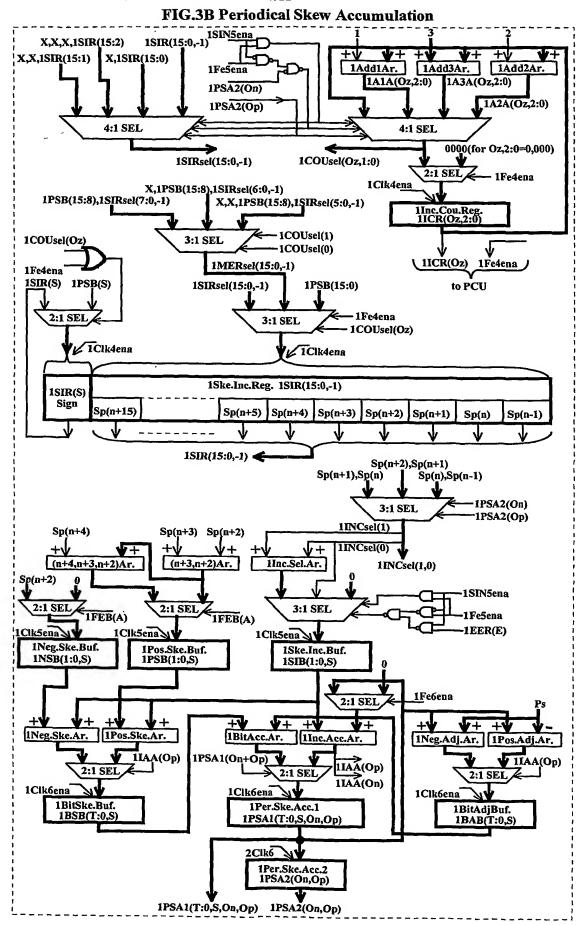
FIG.2D Timing Diagram of Sequential Phase Control proceeded by a phase long data string (continuation of FIG.2C)



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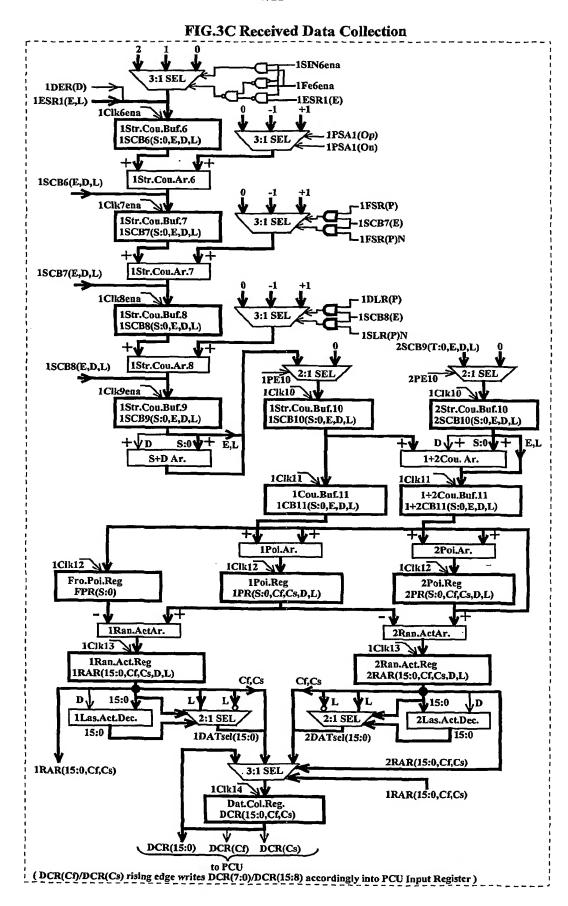
FIG.3A Phase1 of the Phase Processing Stages FCR1(S:0) FMR1(R:0) 11WB(R:0) FCR1(S:0) FMR1(R:0) 12WB(R:0) PCU/QUT(R:0) LD/FMRT \ 11Dig. Filter Arith.1 11DFA1(R:0,Cov) 12Dig. Filter Arith.1 (12DFA1) Filter Mask Reg.1 FMR1(R:0) 11DFAI(Cov) 22DFA1(Cov) 12DFAI(Cov) FMR1(R:0) 11ClkT y (to 21DFR(Cov)) (to 22DFR(Cov)) 12ClkI PCU/OUT(S:0) 12DigitalFilterReg. 12DFR(R:0,Cov) 11DigitalFilterReg. 11DFR(R:0,Cov) LD/FCRI Filter Control Reg.1 FCR2(S:0)FMR2(R:0) FCR2(S:0) FMR2(R:0) FCR1(S:0) 11Dig. Filter Arith.2 12Dig. Filter Arith.2 12DFA2(R:0) FCR1(S:0) 11DFA2(R:0) 11DFA2(R:0) PCU/OUT(R:0) 12DFA2(R:0) LD/FMR2 Filter Mask Reg.2 2:1 SEL, 11SEL-FMR2(R:0) 1DFA(R:0) 1Clk2 FMR2(R:0) 1DigitalFilterReg. 1DFR(R:0) IPCU/OUT(S:0) LD/FCR2 Filter Control Reg.2 FCR2(S:0) 1EndEdgeEncod. 1EEE(T:0,A,L) 1FrontEdgeEncod. 1FEE(T:0,A,L) **▼FCR2(S:0)** 1Clk3 1Clk3 1FEB(T:0,A,L) 2FEB(T:0,A,L) 1 FrontEdgeBuf. 1 EndEdgeBuf. 2FEB(T:0,A,L) 1FEB(T:0,A,L) 1EEB(T:0,A,L) 2EEB(T:0,A,L) 1F/2E - 2:1 SEL 2:1 SEL 1SEsel 2:1 SEL 1SEsel - 1 Ee 1Clk4fro 1Clk4 1Clk4 1 Sec.EdgeReg. 1SER(T:0) 1 FrontEdgeReg. 1 EndEdgeReg. 1EER(T:0,E,L) 1FER(T:0,L) 2:1 SEL 1ENDsel 2:1 SEL 1ENDsel 1Dou.EdgeAr. 1EER(E,L) 1Edg.Ske.Ar.1 A>0 Det. 1Clk5ena 1Edg.Ske.Reg.1 1Clk5ena 1ESR1(T:0,E,L) 1Dou.EdgeReg. 1DER(T:0,D) 1ESR1(E,L) 1Clk6ena 1Edg.Ske.Reg.2 1ESR2(T:0) 1DER(T:0) 1DER(D) 1PSA1(T:0,S,On,Op) 1Fin.Ske.Ar. 1Clk7ena 1Fin.Ske.Reg. 1FSR(T+1:0,P) +1.5Pe -1.5Pe +0.5Pe -0.5Pe 2:1 SEL + 1FSR(P) 2:1 SEL 1FSR(P) 1Dou.Len.Ar. 1Dou.Len.Ar. 1Clk8ena '1Clk8ena 1Dou.Len.Reg. 1Sin.Len.Reg. 1DLR(T+1:0,P) 1SLR(T+1:0,P) $\Psi_{1DLR(P)}$ $\Psi_{1SLR(P)N}$

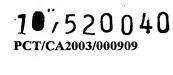
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0/520040







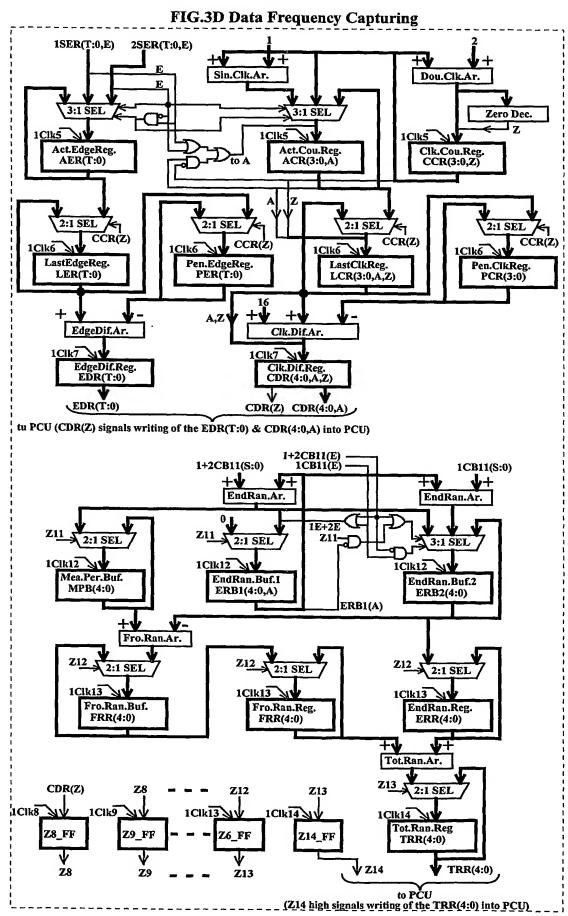
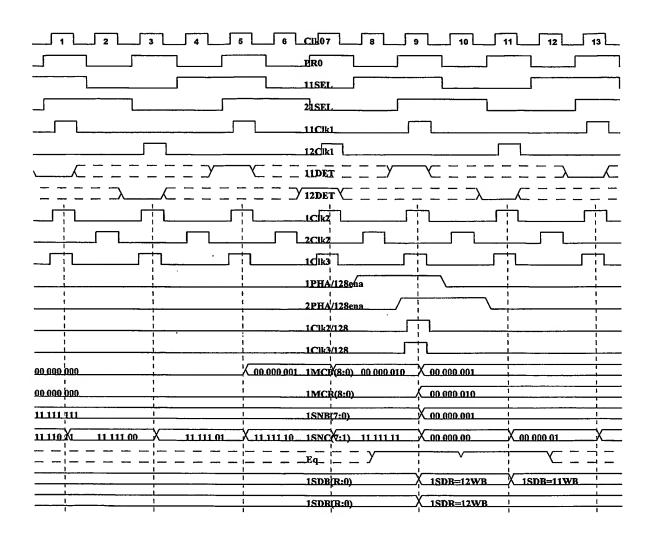


FIG.4A Wave Form Screening & Capturing (WFSC) DCR(P:0) DMR(R:0) 11WB(R:0) DCR(P:0) DMR(R:0) PCU/OUT(R:0) 12WB(R:0) LD/DMR 11MaskDet.Arith. (11MDA) 12MaskDet.Arith. (12MDA) Det. Mask Reg. (DMR) MR(R:0) **∳11DET** V12DET 11SEL PCU/QUT(P:0) 12DET 11DET Add 1 Ar. 11WB(R:0) LD/DCR 11SEL 12DET 12WB(R:0) 2:1 SEL 0 Det.ControlReg. 11DET (DCR) DCR(P:0) 3:1 SEL 3:1 SEL 1Clk2 1PHA/128ena 1Det.DataBuf. 1MaskCou.Buf. 1DDR(R:0) 1MCB(7:0) MCB>0 DEC. 1Clk3/128 1Clk3/128 1Det.DataReg. 1MaskCou.Reg. 1DDR(R:0) 1MCR(7:0,P) 1DDR(R:0) \ 1PHA/128ena 1MCR(7:0) **¥** V1MCR(P) to PCU (1PHA/128ena&1MCR(P)=1 requests the PCU to read the 1DDR(R:0) and 1MCR(7:0)) PRRN PR(R-1) | Clk(R-1) ClkR ERdec 1Clk2 -> Mod. 128 Cou. 1Clk2 QN Zer. Dec. 1Clk2/128 1Clk3/128 1PHA/128ena PR(R-1)N <u>| Clk(</u>R-1) PRR PCU/OUT(7:0) CikR DQ LD/SNR SampleNr.Reg. 2Clk2 QN (SNR) SNR(7:0) 2PHA/128ena 2Clk2/128 2Člk3/128 1SNC(7:1) 1SNB(7:1) 11WB(R:0) SNR(7:0) Sam.Num.Ar. Log.Comp. 1SNB(1)N 12WB(R:0) 1SNB(0)N Eq 2:1 SEL 3:1 SEL (1SNC = 1SNB)1PHA/128ena 1Clk2/128 1Sam.Num.Buf. 1Sam.Num.Cou. 1Sam.DataBuf. 1SNB(7:0) 1SNC(7:1) 1SDB(R:0) 1Clk3/128 1SNB(7:0) 1Sam.DataReg. 1SDR(R:0) 1PHA/128ena 1SDR(R:0) to PCU (1PHA/128ena=1 signals to PCU, that the requested sample is available to be read)

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FIG.4B Timing Diagrams of the WFSC



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